REMARKS

Claims 1, 3, 5, 7, 8, 10, 12, 14 and 22-26 are pending in the present application. Claims 1, 8 and 22 have been amended.

Claim Rejections – 35 U.S.C. 103

Claims 1, 3, 5, 7, 8, 10, 14 and 22-26 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference (U.S. Patent No. 6,201,491) in view of the Ginetti reference (U.S. Patent No. 5,831,566). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The digital-to-analog converting circuit of claim 1 includes in combination among other features a control circuit that "concurrently turns off all of the P-channel type MOS transistors and all of the N-channel type MOS transistors responsive to an externally applied control signal".

The Brunolli et al. reference as primarily relied upon does not disclose the details of a control circuit, and therefore does not disclose or suggest a control circuit that concurrently turns off all switches $S_1 - S_4$ and $S_9 - S_{12}$ shown in Fig. 3, responsive to an externally applied control signal. Moreover, decoder 120 as shown in Fig. 2 of the secondarily relied upon Ginetti reference is not described as concurrently turning off all of switches MN and MP responsive to an externally applied control signal. The prior art as relied upon by the Examiner thus does not inhibit operation of the converting circuit,

so that current consumption is shut off, as in the present invention. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1, 3, 5 and 7, is improper for at least these reasons.

The digital-to-analog converting circuit of claim 8 includes in combination among other features a control circuit "including a plurality of NAND gates that provide respective control signals to the P-channel type MOS transistors and the N-channel type MOS transistors responsive to externally provided bit signals, and that concurrently disable all of the P-channel type MOS transistors and the N-channel type MOS transistors responsive to an externally provided disable signal".

Applicant respectfully submits that the Brunolli et al. and Ginetti references as relied upon do not disclose or suggest a control circuit that concurrently disables all of P-channel type and N-channel type MOS transistors responsive to an externally provided disable signal. Moreover, the Brunolli et al. and Ginetti references do not disclose or suggest a control circuit including a plurality of NAND gates as featured in claim 8. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 8 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 8, 10 and 14, is improper for at least these reasons.

The digital-to-analog converting circuit of claim 22 includes in combination

among other features a control circuit that "concurrently turns off all of the P-channel type MOS transistors and all of the N-channel type MOS transistors responsive to an externally provided disable signal".

Applicant respectfully submits that for at least somewhat similar reasons as set forth above, the Brunolli et al. and Ginetti references do not disclose or suggest a control circuit as featured in claim 22. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 22 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 22-26, is improper for at least these reasons.

Claims 7, 14, 21 and presumably claim 26, have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Brunolli et al. reference and the Ginetti reference, in further view of the Leung et al. reference (U.S. Patent No. 6,400,300). Applicant respectfully submits that the Leung et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the previously relied upon prior art. Applicant therefore respectfully submits that claims 7, 14, 21 and 26 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to these claims, is improper for at least these reasons.

Conclusion

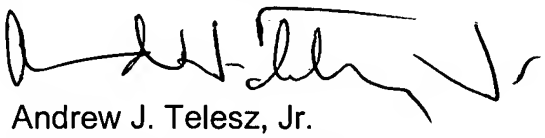
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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